

IN THE DRAWINGS:

Please substitute the attached Replacement Sheets of drawings (4 sheets), which show Figs. 7, 8, 11A through 11D, and 12A through 12C, with the corresponding drawing sheets originally filed showing these figures. In the Replacement Sheets, each of Figs. 7, 8, 11A through 11D, and 12A through 12C have been amended to include the label "PRIOR ART".

Attachments: Replacement Sheets (4 sheets)

REMARKS

The present application has been reviewed in light of the Office Action dated October 20, 2008. A Request for Continued Examination (RCE) Transmittal was filed herewith. Claims 1, 2, and 5-8 are presented for examination, of which Claims 1, 2, and 7 are in independent form. Claim 4 has been cancelled, without prejudice or disclaimer of the subject matter presented therein. Claims 1, 2, and 5-8 have been amended to define aspects of Applicants' invention more clearly. Favorable consideration is requested.

In response to the requirement in the Office Action to amend Figs. 7 and 8 to include the label "PRIOR ART", submitted herewith are four (4) Replacement Sheets of drawings, in which each of Figs. 7, 8, 11A through 11D, and 12A through 12C have been amended to include the label "PRIOR ART". Approval of the amended drawings is respectfully requested.

The Office Action states that Claims 1, 2, and 4-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,791,070 (Hirao et al.). Cancellation of Claim 4 renders its rejection moot. Applicants submit that independent Claims 1, 2, and 7, together with the claims dependent therefrom, are patentably distinct from Hirao et al. for at least the following reasons.

Claim 1 is directed to a photoelectric conversion device that includes a plurality of pixels arranged in a pixel region and a peripheral circuit arranged outside of the pixel region. The plurality of pixels and the peripheral circuit are disposed together on a substrate. Each pixel includes a photoelectric conversion region for converting light into a signal charge. A circuit for

processing the signal charge is included in the peripheral circuit.

The photoelectric conversion region includes first and second semiconductor regions and a transistor. The first semiconductor region is of a first conductivity type and is disposed in the substrate, which is of a second conductivity type that is opposite to the first conductivity type. The second semiconductor region is of the second conductivity type and is disposed in the substrate for accumulating the signal charge. The transistor is configured to transfer the signal charge from the second semiconductor region.

The peripheral circuit includes a third semiconductor region of the first conductivity type disposed in the substrate. An impurity concentration of the first semiconductor region is higher than an impurity concentration of the third semiconductor region, and the first semiconductor region extends deeper into the substrate than the third semiconductor region.

Support for some of the features of Claim 1 may be found, for example, in Fig. 9, in which reference numeral 111 denotes a substrate; reference numeral 110 denotes a first semiconductor region; reference numeral 105 denotes a second semiconductor region; reference numeral 103 denotes a gate electrode of a transfer transistor; and reference numeral 802 denotes a third semiconductor region.²

In the Office Action, it is alleged that Hirao et al. discloses: the first semiconductor region at reference numeral 31 in Fig. 8G; the second semiconductor region at reference numeral 21 in Fig. 8G; and the third semiconductor region at reference numeral 1 in Fig. 8G.

²Any examples presented herein are intended to be used for illustrative purposes and are not to be construed to limit the scope of the claims.

Applicants note, however, that Hirao et al. fails to disclose that the first and third semiconductor regions are of a first conductivity type and are disposed in a substrate of a second conductivity type that is opposite to the first conductivity type. Additionally, Hirao et al. fails to disclose or suggest that the second semiconductor region is part of a photoelectric conversion region that includes a transistor for transferring signal charge from the second semiconductor region. It is respectfully submitted that one of ordinary skill in the art would not find the structural arrangement claimed in Claim 1 to be obvious in view of the disclosure of Hirao et al.

Furthermore, Hirao et al. fails to teach or suggest a peripheral circuit, as claimed in claim 1, in which the peripheral circuit includes a third semiconductor region of the first conductivity type disposed in the substrate, in which an impurity concentration of the first semiconductor region is higher than an impurity concentration of the third semiconductor region, and in which the first semiconductor region extends deeper into the substrate than the third semiconductor region. Applicants note that, even if reference numeral 20 in Fig. 8G of Hirao et al. could be considered to correspond to the third semiconductor region of Claim 1, nothing in Hirao et al. would even suggest what the depth and the impurity concentration of that portion of Hirao et al. (i.e., the portion denoted by reference numeral 20) would be.

In summary, nothing has been found in Hirao et al. that is believed to teach or suggest a photoelectric conversion device that includes a plurality of pixels arranged in a pixel region, each pixel including a photoelectric conversion region for converting light into a signal charge, and a peripheral circuit arranged outside of the pixel region and including a circuit for processing the signal charge, the plurality of pixels and the peripheral circuit being disposed

together on a substrate, wherein "the photoelectric conversion region includes: a first semiconductor region of a first conductivity type disposed in the substrate of a second conductivity type that is opposite to the first conductivity type; a second semiconductor region of the second conductivity type that is opposite to the first conductivity type, the second semiconductor region being disposed in the first semiconductor region for accumulating the signal charge; and a transistor for transferring the signal charge, the transistor being disposed in the first semiconductor region," wherein "the peripheral circuit includes a third semiconductor region of the first conductivity type disposed in the substrate of the second conductivity type," wherein "an impurity concentration of the first semiconductor region is higher than an impurity concentration of the third semiconductor region," and wherein "the first semiconductor region extends deeper into the substrate than the third semiconductor region," as recited in Claim 1. Accordingly, Applicants submit that Claim 1 is patentable over Hirao et al. and respectfully request withdrawal of the rejection under 35 U.S.C. § 103(a).

Independent Claims 2 and 7 include features similar to those of Claim 1, and are believed to be patentable for at least the reasons discussed above. Additionally, the other claims in the present application depend from one or another of Claims 1, 2, and 7, and are submitted to be patentable for at least the same reasons. However, because each dependent claim also is deemed to define an additional aspect of the invention, individual consideration of the patentability of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable consideration and an early passage to issue of the present application.

No petition to extend the time for response to the Office Action is deemed necessary for this Amendment. If, however, such a petition is required to make this Amendment timely filed, then this paper should be considered such a petition and the Commissioner is authorized to charge the requisite petition fee to Deposit Account 50-3939.

Applicants' undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

/Lock See Yu-Jahnes/
Lock See Yu-Jahnes
Attorney for Applicants
Registration No. 38,667

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200